

**Project 1**

**Counter with Display**

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**Introduction:**

This project will use eight LED’s on the board to display the count. A momentary switch is used for both incrementing and decrementing the counter as well as reset. A slide switch implemented and will increment when up (1) and when off (0) it will decrement. Four main modules are instantiated in the top level. Mainly the AISO will generate a reset signal for resetting all logic within the design. In addition, a pulse maker will detect the rising edge and generate the necessary clock wide pulse of 10ms.

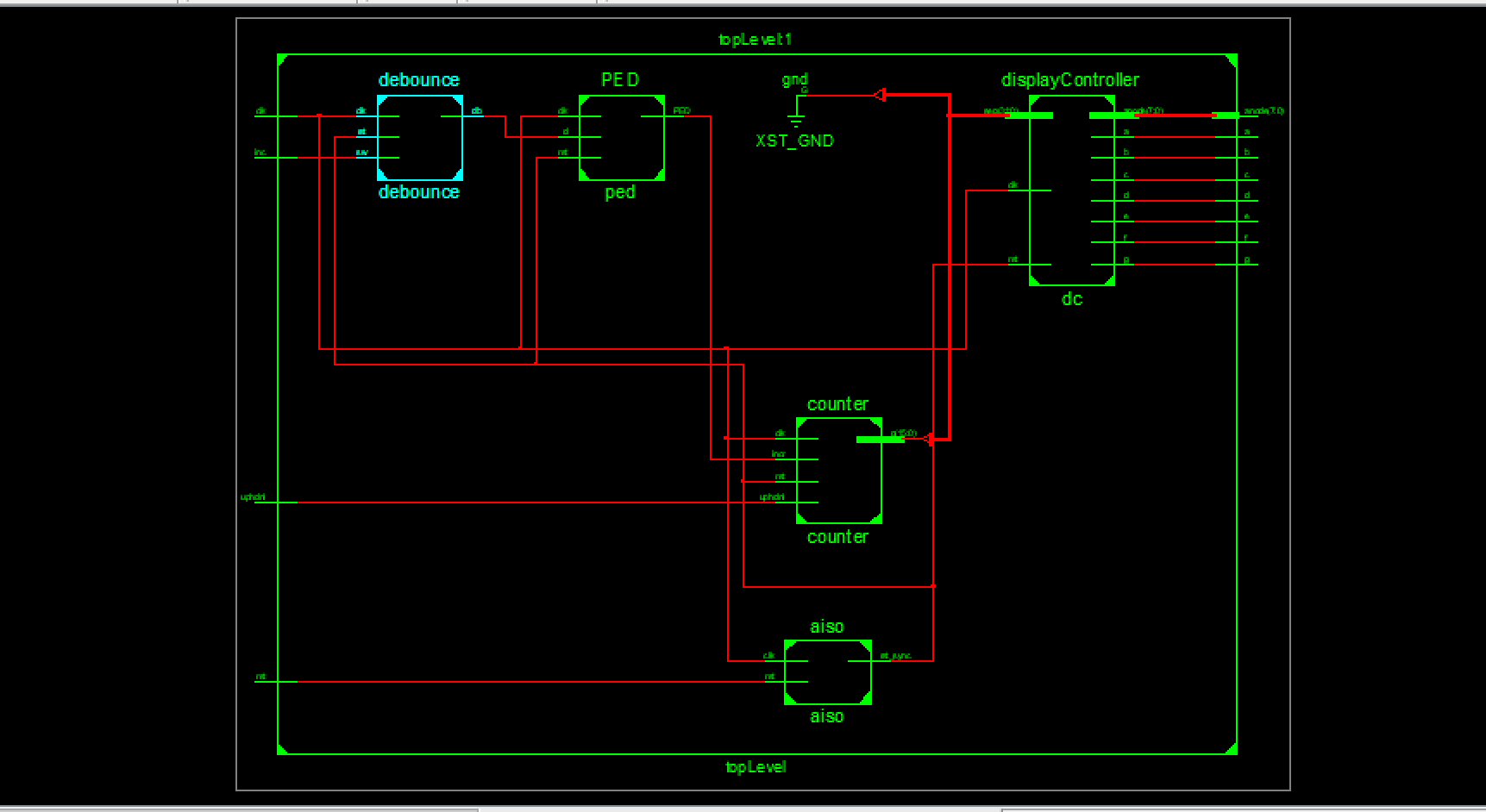
**Functional Blocks Description:**

* Debounce: Debounce will stabilize the output to show only the necessary transitions.
  + Pulse Maker: This module makes a pulse every 10ms.
* AISO: This module helps with the violation of timing constraints. AISO: Asynchronous In Synchronous Out
* PED: This module will detect the positive edge of the clock specifically as an output. The output can only change on the positive edge detect.
* Counter: Will increment / decrement based on the switch uphdnl. This is the module where incrementing and decrementing is done based on the condition of the switch. The switch is set as “Up High Down Low”.
* Display Controller: This module instantiates the modules required for the 7 segment display.
* This is the module where the 7-segment module is instantiated and controlled using led clock, led controller, ad mux, and hex to 7 segment.
  + Led Clock: Integer count determines frequency of clkOut. So count = (incoming frequency / outgoing frequency) / 2. ClkIn which is 100Mhz alternates ‘count’ in which clkOut will also alternates. We want an output of 480Hz frequency to have a rate of 60Hz refresh, which is determined by outgoing frequency = refresh rate \* number of pixels.
  + Led Controller: This module has an input clock because at the posedge of the clock, our Moore FSM increment to next state regardless of the value. The output will be in relation to the analog pins {a7-aa0} and the present state {segSel}. Pixel are on from right to left of the display.
  + Ad Mux: This module is an eight to 1 mux that has a select bit of 3 bits.
  + Hex to 7 Segment: This module will change hex value inputs to be able to use with the seven segment display of the Nexys 4.
* topLevelUCF: This is the module where all the blocks are linked to the NEXYS 4 board.

**Project 1 Hierarchy:**

* topLevel
  + debounce
    - makePulse
  + aiso
  + PED
  + counter
  + displayController
    - ledClk
    - ledController
    - adMux
    - Hex7seg
  + topLevelUCF

**RTL Schematic:**



**Conclusion:**

The use of the debounce module was vital to the project due to that it stabilizes the output of the clock, showing us only the necessary transition. The debounce was modeled after Pong Chu’s. The AISO module help us prevent violating the timing constraints and thus creating a counter to decrement when switch is low (0) and increment when switch is high (1). The counter is able to display on our Nexys 4 board due to the module display controller, displaying the 8 or 16 bit values on the LCD.